AMENDMENTS TO THE SPECIFICATION

Please replace the paragraphs on page 4, lines 17-24 with the following amended paragraphs:

FIG. [[4A]] 4 is diagram illustrating a transaction cell constructed according to one embodiment of the present invention that is used to route data within the multiple processor device of FIG. 2;

FIG. [[4B]] 5 is a diagram illustrating an agent status information table constructed according to an embodiment of the present invention that is used to schedule the routing of transaction cells within the multiple processor device of FIG. 2;

~~FIG. 5 is a graphical representation of transporting data between devices in accordance with the present invention;~~

Please replace the paragraphs on page 5, lines 10-13 with the following amended paragraphs:

FIG. 13 is an illustration of the interaction between the packet manager, a receiver, and a transmitter for transferring data in the system of the present invention ~~a flow chart illustrating operation of the switching module in servicing agents to transfer transaction cells between the agents~~.

FIG. 14 is a flowchart illustrating operation of the switching module in servicing agents to transfer transaction cells between the agents ~~an illustration of the interaction between the packet manager, a receiver, and a transmitter for transferring data in the system of the present invention~~.

Please replace the paragraph on page 12, lines 18-30 with the following amended paragraph:

FIG. 6 further illustrates an example of the processing performed by the Rx MAC module 60 or 66. In the example, data segment 1 of the received stream of data 92 corresponds with control information CNTL 1. The elastic storage device 80 stores data segment 1, which, with respect to the Rx MAC module 60 or 66, is a set number of bytes of data (e.g., 8 bytes, 16 bytes, etc.). The decoder module 82 decodes data segment 1 to determine that data segment 1 corresponds to control information. The decoded data segment is then stored in the reassembly buffer 84 or provided to the receiver buffer 88. If the decoded control information segment is provided to the reassembly buffer 84, it is stored in a first-in-first-out manner. At some later time, the decoded control information segment is read from the reassembly buffer 84 by the routing module 86 and interpreted to determine that it is control information associated with a particular packet or particular control function. Based on this interpretation, the decoded data segment 1 is stored in a particular location of the receiver buffer 88.

Please replace the paragraph beginning on page 13, lines 32- page 14, line 9 with the following amended paragraph:

FIG. 7 is a graphical representation of the function of the Tx MAC module 58 or 68 and the Rx MAC module 60 or 66. The Tx MAC module 58 or 68 receives packets from a plurality of output virtual channels via the switching module 51. FIG. 7 illustrates the packets received by the Tx MAC module 58 or 68 from a first virtual channel (VC1). The data is shown in a generic format, which may correspond to ATM cells, frame relay packets, IP packets, TCP/IP packets, other types of packet switched formatting, and/or circuit switched formatting. The Tx MAC module 58 or 68 partitions the generically formatted packets into a plurality of data segments of a particular size. For example, the first data packet of virtual channel 1 is partitioned into three segments, VC1_A, VC1_B, and VC1_C. The particular size of the data segments corresponds with the desired data path size, which may be 8 bytes, 16 bytes, etc.